UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,055	09/24/2001	Masaaki Hiroki	740756-2367	6718

31780 7590 10/12/2006

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/961,055	HIROKI ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2006 and 02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,6-9,19,21,24-42 and 44-58* is/are pending in the application.

4a) Of the above claim(s) *24-36 and 48-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,6-9,19,21,37-42 and 44-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/837,394.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 31, 2006 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 4, 6-9,19, 21,37-42, and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,051,570 (Tsujikawa et al) in view of US 4,007,294 (Woods et al), and further in view of US 4,778,258 (Parks et al).

Regarding claims 2,4,6-9 and 37-42, **Tsujikawa** teaches (col.10, line 36 – col.11, line 39; Fig. 9) an electro-optical display device comprising:

(concerning claim 2, 37)

- a first substrate (128) having an insulating surface (glass substrate);
- at least one thin film transistor (103,104) formed over the first substrate (128), the thin film transistor (103,104) having channel region, source and drain

regions, such as electrodes (117,118) with the channel region extending therebetween, a gate insulating film (134,135) adjacent to the channel region, and a gate electrode (112,113) adjacent the gate insulating film (134,135);

- a leveling film (123) comprising organic resin formed over the at least one thin film transistor (103,104), because the interlayer insulating film (123) formed of polyimide (organic resin) and functions as flatten the surface as shown in the Fig.9;
- a pixel electrode (124) formed over the leveling film (123) and electrically connected to the source region or drain region of the thin film transistor (103,104) as shown in Fig.9;

(concerning claims 4, 38)

- an interlayer insulating film (122) formed over the thin film transistor (103,104);
- an electrode (such as 118) formed on the interlayer insulating film (122) and electrically connected to the source region or drain region;
- a pixel electrode (124) formed over the leveling film (123) and electrically connected to the source region or drain region of the thin film transistor (103,104) through the electrode (118) as shown in Fig.9;

(concerning claims 6, 7, 39, 40)

- a gate insulating film (134,135) over the channel region, and the gate electrode (112, 113) over the gate insulating film (134,135);

(concerning claims 8, 9, 41, 42)

- an electrode (such as 118) electrically connected to the source region or drain region through a first contact hole of the interlayer insulating film (122) as shown in Fig.9;
- the pixel electrode (124) contacts the electrode (118) through a second contact hole of the leveling film (123) as shown in Fig.9;
- the second contact hole does not overlap the first contact hole as shown in Fig.9;

(concerning claims 37-42)

- the electro-optical display having an active matrix type display can be used in any electronic device such as camera in the preamble of the claims that are only given weight as intended use, and that would have been at least obvious.

Tsujikawa further teaches that the gate insulating film is formed of silicon oxide (see col.8, lines 16-18 that is the same as shown in the Fig.9 of the gate insulating film 134,135), but Tsujikawa does not explicitly teach that the gate insulating film contains fluorine and the pixel electrode is transparent.

Woods teaches (abstract) that a method of treating a layer of silicon dioxide in which an fluoride compound is applied to one surface of the silicon dioxide layer to prevent the deleterious effect resulting from any mobile impurity ions therein, so that would obtain more protection.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the electro-optical display device of Tsujikawa with the

teachings of the gate insulating film having fluorine as taught by Woods, since the skilled in the art would be motivated for preventing the deleterious effect resulting from any mobile impurity ions therein (abstract).

Tsujikawa and Woods teach the invention set forth above except for that the pixel electrode is transparent.

Parks teaches (col.5, lines 15-20) in general, pixel electrode having transparent material (transparent pixel electrode), and that is particularly useful in LCD displays in which back lighting is employed to form or assist in forming the desired image.

Therefore, it would have been obvious to those skilled in the art at time the invention was made to modify the electro-optical display device of Tsujikawa and film treatment of Woods with the teachings of using transparent pixel electrode as taught by Parks, since the skilled in the art would be motivated for achieving a desired image, particularly, for the transmission type liquid crystal display as indicated in paragraph 0147 of this application.

Regarding claims 19 and 44, Tsujikawa teaches (col.11, lines 18-23; Fig.9) that the liquid crystal (125) is disposed between the first substrate (128) and the second substrate (127).

Regarding claims 21 and 45, Tsujikawa teaches (col.11, lines 30-33; Fig.9) that the leveling film (123) comprises polyimide, because the interlayer insulating film (123) functions as flatten the surface as shown in the Fig.9, such that the interlayer insulating film (123) is a leveling film.

Regarding claim 46, Tsujikawa teaches (col.10, lines 43-55;Fig.9) that the channel region (between the source region and the drain region of the thin film transistor) comprises crystalline silicon.

Regarding claim 47, Tsujikawa teaches (col.8, line 16-18) the gate insulating film comprises silicon oxide (the Fig.6 shows the same as the Fig.9 for the gate insulating film 134, 135).

Response to Arguments

3. Applicant's arguments filed on June.2, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument that the references cannot be combined, it is point out in Tsujikawa reference teaches (col.11, lines 30-33; Fig.9) that the leveling film (123) comprises polyimide, because the interlayer insulating film (123) functions as flatten the surface as shown in the Fig.9, such that the interlayer insulating film (123) is a leveling film. Even thought the pixel electrode in Tsujikawa using reflective electrode, using transparent pixel electrode in transmission type liquid crystal display that is common and known in the art. As evidence Parks teaches (col.5, lines 15-20) in general, pixel electrode having transparent material (transparent pixel electrode), and that is particularly useful in LCD displays in which back lighting is employed to form or assist in forming the desired image.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MQ

Mike Qi
Patent examiner
Sep. 26, 2006